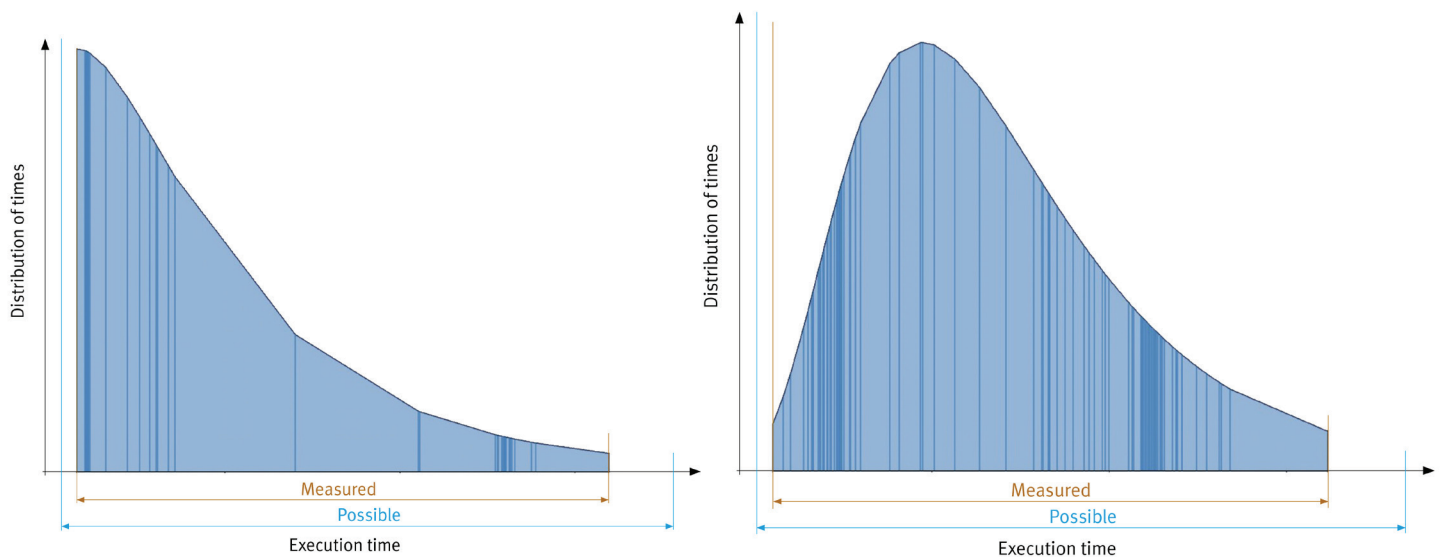


TBwcet – Worst Case Execution Timing by measurement

LDRA, leader in standards compliance, automated software verification, software code analysis and test tools, maintains its commitment to supporting the development of critical embedded software systems with the introduction of TBwcet.

Real-time, closed-loop control systems across the sectors rely on the deterministic completion of defined tasks within tight time windows to gather data, process it, and update the system. That places the onus on developers to ensure that the completion of these tasks is achievable even in the worst case. When multicore processors are involved interference channels resulting from shared resources make theoretical calculations insoluble. The only way to provide evidence of adequate resourcing and mitigation for interference is by measuring worst case execution times (WCET) on the target.

TBwcet addresses the resource usage evaluation demands of automotive standard ISO 26262, and other functional safety standards. WCET analysis is also specified for aviation applications in CAST-32A and A(M)C 20-193, and these also demand data and control coupling coverage to highlight possible interference scenarios. Appropriate coupling coverage analysis is also supported by the LDRA tool suite.



TBwcet timing diagram without interference

TBwcet timing diagram with interference

TBwcet complements the proven technology of unit testing and the [TBrun component of the LDRA tool suite](#). The tool automates the measurements, running the specified tests repeatedly and providing a graphical representation of the variation in execution times. It provides a facility for processor cores to be loaded to varying degrees, which in turn loads shared resources too.

The result is an ideal platform to perform interference research, and to ultimately demonstrate that the resulting interference mitigation ensures that WCET verification requirements are met.

Guided by static analysis...

It is not possible to calculate WCETs for multicore applications. However, static analysis does have a contribution to make to a more precise, reliable approach.

There are long standing and proven mechanisms available to measure the properties of software code which are independent of their execution on any particular platform. For example, the [TBvision component of the LDRA tool suite](#) can precisely calculate [Halstead's metrics](#) which reflect software module size, software complexity, and the data flow information.

Halsteads (Cashregister.c)

File	Total Operators	Total Operands	Unique Operators	Unique Operands	Vocabulary	Length	Volume
Total for Cashregister.c	149	230	16	56	72	379	2338

Such an approach can identify which sections of code are the most demanding of processing time and can yield call diagrams associated with the code base.

...and proven by dynamic analysis

The information derived from static analysis provides valuable focus on the most demanding execution paths in the software for the subsequent measurement of execution times in the target environment using TBrun and TBwcet.

The screenshot displays the LDRA tool suite interface with several panels:

- Log View:** Shows the sequence selected (TCI_1_1_2) and the process of assigning, resolving, and optimising stubs.
- File View:** Displays the sequence file explorer with the file `image_blur.c` selected.
- Calls View:** A table showing procedure calls and their frequencies.
- Test Case View:** A table showing test cases, including `tc_1 (100 Reps)` for the `blur` procedure.
- Variable I/O View:** Shows variables like `ldra.bmp`, `ldra_blur.bmp`, `1`, and `ldra_qq_duration`.
- Driver Build & Execution Options:** A dialog box for configuring the build and execution environment.

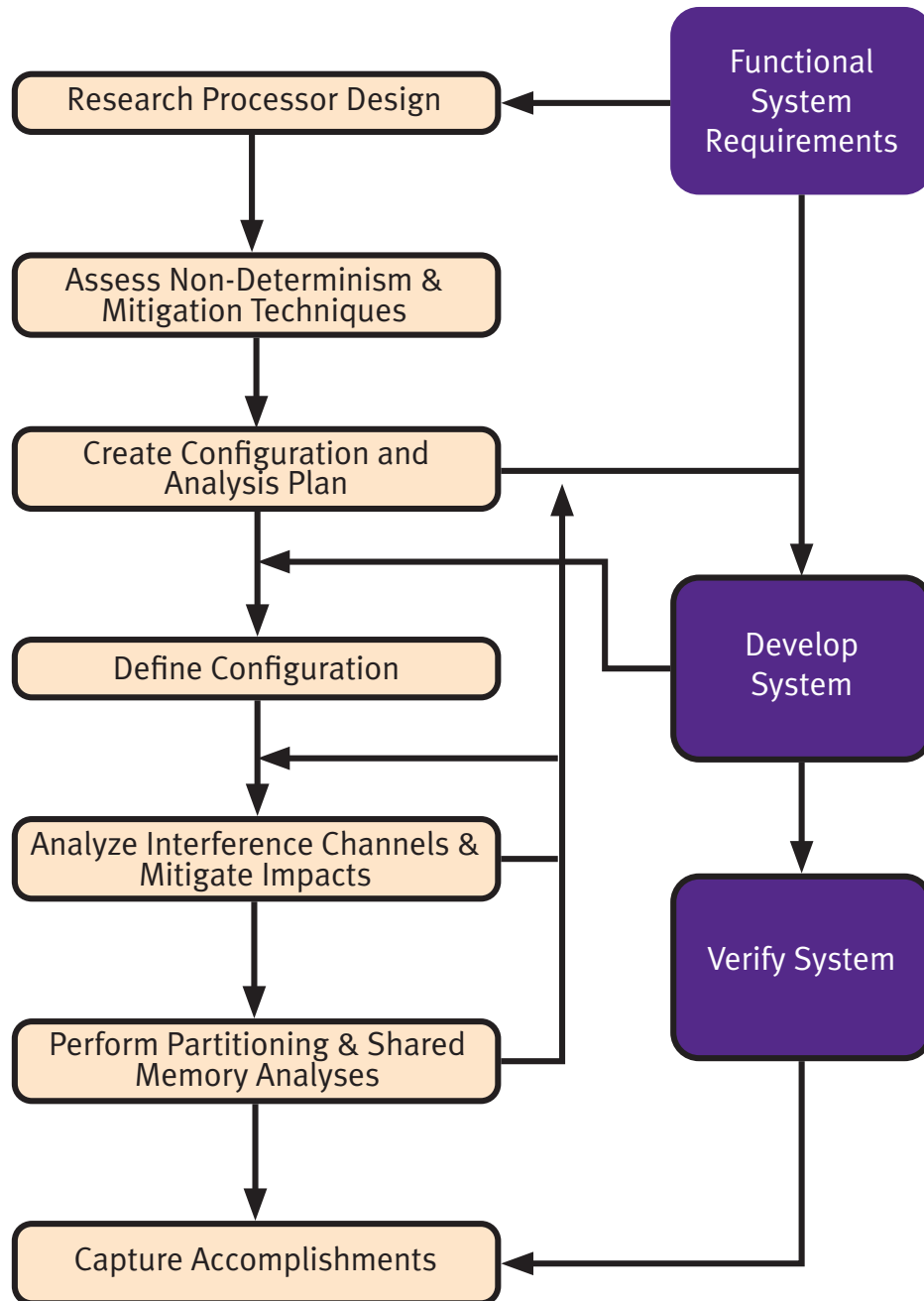
The **Driver Build & Execution Options** dialog box is currently open, showing the **Execution** tab. It contains the following fields:

- Executable Name:** `$(Seqworkdir)$($SeqName)_$(ProgFullID)$($ExeExtension)`
- Execution Command:** `run_wcet_remote.sh "$($Exe)" stress= 1`

The LDRA tool suite measures WCET dynamically, timing the performance of each complete-cycle algorithm in turn on a running system. It includes the capability to load one or more cores, and forces hardware interference to play a part by repeatedly executing WCET tests.

Interference research and iterative development

The empirical nature of verification and validation in the multiprocessor environment makes it imperative that project managers can adapt to changing requirements and configurations. The iterative nature of the interference research process used to mitigate for interference makes feedback loops a necessary part of the development process. Support for the use of a simulator allows tests to be developed even without the use of target hardware.



It is highly likely that such interference research will lead to changes in system or software requirements, and conversely that changes in system functional requirements will drive new interference channels or affect existing ones. The automated traceability provided by the [TBmanager component of the LDRA tool suite](#) is invaluable for keeping track of the need for repeat verification and validation activities.

Benefits

- intuitive mechanism for the measurement of execution times on-target
- configurable to allow focus of analysis on a task-by-task basis
- variable resource stress levels to show the effect of interference and its mitigation
- supports almost any target device*
- graphical representation of execution times provides instant feedback
- provides test platform for interference research, supported by automated requirements traceability
- static analysis provides focus for interference research
- presents evidence of adequate mitigation for interference
- supports the fulfillment of WCET related objectives in CAST-32A, A(M)C 20-193, and ISO 26262, and other functional safety standards

Solution details

- TBwcet builds upon proven TBrun unit test technology, used in hundreds of certifications
- TBwcet is supplemental to the LDRA tool suite, making it easy to integrate as part of the project-wide solution
- Evidential artefacts are appropriate for submission in support of functional safety and cybersecurity standards compliance
- Hardware interfaces to target devices* are supported by means of Target License Packages (TLPs)
- Instrumentation for timing analysis is optimized to ensure negligible impact on task execution times
- Supports applications with or without the provision of robust partitioning
- Complements LDRA tool suite's Data and Control coupling coverage to provide an extensive solution to the challenges posed by CAST-32A and A(M)C 20-193

Conclusion

TBwcet complements TBrun to leverage LDRA's industry leading unit test, integration test, and coverage analysis technologies. It draws on the company's expertise as exemplified by its leading role in the creation of process, functional safety, and coding standards including DO-178C, ISO 26262, FACE, MISRA C, MISRA C++, JSF++ AV, CERT C, and CERT C++.

LDRA's products and services are widely used by companies whose names are synonymous with embedded electronic systems across a wide range of industrial sectors. The LDRA tool suite is SGS TÜV Saar certified and complies with the demands of IEC 61508, IEC 62304, IEC 60880, EN 50128 and ISO 26262, and the company's Quality Management System is certified in accordance with ISO 9001:2015.

* Contact LDRA for further information relating to your tool chain



LDRA
LDRA UK & Worldwide
Portside, Monks Ferry,
Wirral, CH41 5LH
Tel: +44 (0)151 649 9300
e-mail: info@ldra.com

LDRA Technology Inc.
2540 King Arthur Blvd, Suite 228
Lewisville, Texas 75056
United States
Tel: +1 (855) 855 5372
e-mail: info@ldra.com
LDRA Technology Pvt. Ltd.
Unit B-3, Third floor Tower B, Golden Enclave,
HAL Airport Road, Bengaluru, 560017
Tel: +91 80 4080 8707
e-mail: india@ldra.com